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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/767,069	01/30/2004	Shoji Shukuri	501.42645VX1	5443

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EXAMINER	
NHU, DAVID	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 12/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/767,069	SHUKURI, SHOJI	
	Examiner	Art Unit	
	David Nhu	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-85* is/are pending in the application.

4a) Of the above claim(s) *1-51,58-62 and 75-85* is/are withdrawn from consideration.

5)☒ Claim(s) *63-67 and 71-74* is/are allowed.

6)☒ Claim(s) *52-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/400,469.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTIONS

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claims 52-57 are rejected under 35 U.S.C. 102(e) as being anticipated by Shimizu et al (6,555,427 B1).

Regarding claim 52, Shimizu, (see figures 32A-32D, 33A-33F, 34A-34F, 35A-35B, col. 27, lines 45-67, col. 28, lines 1-65), teaches a method of manufacturing a semiconductor integrated circuit device, comprising steps of: forming a first conductive film 83 over a memory cell forming region and a peripheral circuit transistor forming region of a semiconductor substrate 81; patterning said first conductive film lying over the memory cell region to form a first conductive pattern which serves as a first gate electrode 83 of a memory cell and leaving said first conductive film over said peripheral circuit transistor region; forming a second conductive film 87 over said memory cell region and said first conductive film in said peripheral circuit transistor region; and etching said second conductive film to form each second gate electrode 87 of said memory cell on at least side walls of said first conductive pattern, and forming a gate electrode 88 of each peripheral circuit transistor comprising said second conductive film and first conductive film over said peripheral transistor region.

Regarding to claims 53-57, Shimizu, col. 1-34, also teach wherein said memory cell includes, in a memory cell forming region of said semiconductor substrate, a source region, a drain region, a channel region interposed between said source region and said drain region, a control gate electrode and a memory gate electrode disposed over said channel region, a first gate insulating film 28 form between said channel region and said control gate electrode 29, and a charge storage region 27 formed between said channel region and said memory gate electrode (see figures 23D, 33F, 34F, 35A-35B), wherein said first gate electrode constitutes said control gate electrode, and wherein said second gate electrode constitutes said memory gate electrode; wherein said peripheral circuit transistors include a low withstand voltage transistor operated at a power voltage, and a high withstand voltage transistor operated at a voltage higher than said power voltage (see figures 33A-33F, 34A-34F, 35A-35B); wherein said second gate electrode is formed on side walls of said first gate electrode through an insulating film in sidewall spacer (see figure 9A-9C); wherein an electrode withdrawal portion of said second gate electrode is formed in said forming step of the second gate electrode; patterning said first conductive pattern after said formation of the second gate electrode to thereby form said first gate electrode.

Allowable Subject Matter

3. Claims 63-67, 71-74 are allowed.

The following is a statement of reason for the indication of allowance subject matter: Shimizu fails to teach forming sidewall spacers, each comprised of an insulating film, in self-alignment with said walls of said second gate electrode; forming a silicide layer for each of said first conductive pattern and said second gate electrode in self-alignment with respect to said

sidewall spacers; etching said first conductive pattern in self-alignment with respect to said sidewall spacers to form corresponding first gate electrode.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Shimizu'508, Kim'642, Park'399, Kwon'311, Shimizu'611, Choi'749 are cited as of interest.

5. A shortened statutory period for response to this action is set to expired 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned(see 710.02 (b)).

6. Any inquiry concerning this communication on earlier communications from the examiner should be directed to David Nhu (571)272-1792. The examiner can normally be reached on Monday-Friday from 7:30 AM to 5:00 PM. The examiner's supervisor, David Nelms can be reached on (571)272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the patent application information retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David Nhu

December 14, 2004